UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/679,000	10/02/2003	Robert C. Chang	SANDP039	8920

10027 7590 10/20/2006

ANDERSON, LEVINE & LINTEL L.L.P.
14785 PRESTON ROAD
SUITE 650
DALLAS, TX 75254

EXAMINER	
TSAI, SHENG JEN	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 10/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)
	10/679,000	CHANG ET AL.
	Examiner	Art Unit
	Sheng-Jen Tsai	2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25 and 27-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is taken in response to Applicant's Amendments and Remarks filed on 10/10/2006 regarding application 10,679,000 filed on 10/02/2003.

2. Claims 1-25 and 17-31 are pending for consideration.

3. ***Response to Amendments and Remarks***

Applicant's amendments and remarks have been fully and carefully considered.

In response, a new ground of claim analysis based on a newly identified reference (Bassett et al., US 6,747,827) in combination of previously cited references has been made. Refer to the corresponding sections of the claim analysis for details.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1, 3-4, 6-7, 10-11, 15, 21, 23, 27-28 and 31 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 3 and 10 of copending Application No. **10/678,893**, as shown in the following table. Although not all of the conflicting claims are exactly identical, they are extremely similar and are not patentably distinct from each other, as explained in the "explanation" section below.

10/679,000	**10/678,893**
1. (currently amended) A method for encoding data associated with a page within a non-volatile memory of a memory system, the page having a data area and an overhead area, the method comprising: dividing at least a part of the page into at least two segments of the data, the at least two segments of the data including a first segment and a second segment; performing error correction code (ECC) calculations on the first segment according to a first ECC algorithm to encode the first segment; and performing the ECC calculations on the second segment according to a second ECC algorithm to encode the second segment, wherein the second segment is encoded substantially separately from the first segment.	1. (currently amended) A method for storing data within a non-volatile memory comprising a plurality of blocks in an array formed on a semiconductor substrate, each of the plurality of blocks having an indicator indicative of reliability of that block, the method comprising: identifying a first block of the plurality of blocks into which the data is to be stored; responsive to the indicator associated with the first block meeting a criterion, encoding the data using a first error detection algorithm; then writing the encoded data into the first block; identifying a second block of the plurality of blocks into which the data is to be stored; responsive to the indicator associated with the second block not meeting the criterion, encoding the data using a second error detection algorithm; the second error detection algorithm having a higher error detection capability than the first error detection algorithm; and then writing the encoded data into the second block;
2. The method of claim 1 wherein the first segment includes the data area and the second segment includes the overhead area.	3. The method of claim 1 wherein the first error detection algorithm is a 1-bit error detection code (ECC) algorithm and the second algorithm is a 2-bit ECC algorithm.
3. The method of claim 1 wherein the first segment includes a first section of the data area and the second segment includes a second section of the data area.	9. The method of claim 1 wherein the non-volatile memory is a flash memory.
4. The method of claim 1 wherein the first ECC calculations are associated with an ECC algorithm that is arranged to detect up to two incorrect bits and to correct up to one of the incorrect bits in each	10. The method of claim 9 wherein the flash memory is one of a NAND flash memory and an MLC NAND flash memory.

of the first segment and the second segment.	
5. The method of claim 4 wherein the first ECC algorithm is a Hamming Code ECC algorithm.	
6. The method of claim 1 wherein dividing the at least part of the page into the at least two segments of the data includes: dividing the page into three segments, the three segments including the first segment, the second segment, and a third segment.	
7. The method of claim 6 further including: performing the ECC calculations on the third segment to encode the third segment, wherein the third segment is encoded substantially separately from the first segment and the second segment.	
8. The method of claim 6 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes the overhead area.	
9. The method of claim 6 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes a third section of the data area.	
10. The method of claim 1 wherein the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.	
11. A memory system comprising: a non-volatile memory, the non-volatile memory including a page, the page having a data area and an overhead area, the data area and the overhead area being arranged to contain bits of data; code devices for dividing at least a part of the page into at least two segments, the at least two segments including a first segment and a second segment; code devices for performing error correction code (ECC) calculations on the first segment according to a first ECC algorithm to encode the first segment and on the second segment according to a second ECC algorithm to encode the second segment, wherein the second segment is encoded substantially separately from the first segment; and a memory area for storing the code devices.	
12. The memory system of claim 11 further including: a controller, the controller being arranged to process the code devices.	
13. The memory system of claim 11 wherein the first segment includes the data area and the second segment includes the overhead area.	

14. The memory system of claim 11 wherein the first segment includes a first section of the data area and the second segment includes a second section of the data area.	
15. The memory system of claim 11 wherein the first ECC calculations are associated with an ECC algorithm that is arranged to detect up to two incorrect bits and to correct up to one of the incorrect bits in each of the first segment and the second segment.	
16. The memory system of claim 15 wherein the first ECC algorithm is a Hamming Code ECC algorithm.	
17. The memory system of claim 11 wherein the code devices for dividing the at least part of the page into the at least two segments include: code devices for dividing the page into three segments, the three segments including the first segment, the second segment, and a third segment.	
18. The memory system of claim 17 further including: code devices for performing the ECC calculations on the third segment according to one of the first and second ECC algorithm to encode the third segment, wherein the third segment is encoded substantially separately from the first segment and the second segment.	
19. The memory system of claim 17 wherein the first segment includes a first section of the data area, the third segment includes a second section of the data area, and the second segment includes the overhead area.	
20. The memory system of claim 17 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes a third section of the data area.	
21. The memory system of claim 11 wherein the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.	
22. The memory system of claim 11 wherein the code devices are one of software code devices and firmware code devices.	
23. A memory system comprising: a non-volatile memory, the non-volatile memory including a page, the page having a data area and an overhead area, the data area and the overhead area being arranged to contain bits of data; means that divide at least a part of the page into at least two segments, the at least two segments including a first segment and a second segment; and means	

that perform error correction code (ECC) calculations on the first segment according to a first ECC algorithm to encode the first segment and on the second segment according to a second ECC algorithm to encode the second segment, wherein the second segment is encoded substantially separately from the first segment.	
24. The memory system of claim 23 wherein the first segment includes the data area and the second segment includes the overhead area.	
25. The memory system of claim 23 wherein the first segment includes a first section of the data area and the second segment includes a second section of the data area.	
27. The memory system of claim 23 wherein the means that divide the at least part of the page into the at least two segments include: means that divide the page into three segments, the three segments including the first segment, the second segment, and a third segment.	
28. The memory system of claim 27 further including: means that perform the ECC calculations according to one of the first and second ECC algorithms on the third segment to encode the third segment, wherein the third segment is encoded substantially separately from the first segment and the second segment.	
29. The memory system of claim 27 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes the overhead area.	
30. The memory system of claim 27 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes a third section of the data area.	
31. The memory system of claim 23 wherein the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.	

10/679,000	10/678,893	EXPLANATION
1, 11 and 23	1	Both describe applying a first ECC algorithm to a first segment and a second ECC algorithm to a second segment of a non-volatile memory
3 and 15	3	Both recite a ECC algorithm that detects up to two incorrect bits and corrects up to one incorrect bit
6, 7, 27 and 28	1	Both recite the presence of a plurality of segments and the applications of ECC algorithm to each segment
10, 21 and 31	10	Both recite that the non-volatile memory is of NAND flash memory and MLC NAND flash memory

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-3, 6-9, 11-14, 17-20, 22-25 and 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith (US 6,961,890), and in view of Bassett et al. (US 6,747,827).

As to claim 1, Smith discloses **a method for encoding data associated with a page within a non-volatile memory of a memory system** [Dynamic Variable-Length Error Correction Code (title; abstract)], the page having a data area and an overhead area, the method comprising:

dividing at least a part of the page into at least two segments of the data, the at least two segments of the data including a first segment and a second segment [a divider segregating the payload and redundancy portions may be dynamically relocated, thereby altering the size of the redundancy to allow for use of an error correcting code selected to provide the data integrity required in response to changing conditions (abstract); figures 1 and 2 show the dividing of a memory page into a plurality of segments (206, 208, 210 and 212); column 4, lines 16-31];

performing error correction code (ECC) calculations on the first segment according to a first ECC algorithm to encode the first segment [The fundamental error rate is particularly dependent upon factors that are a function of time. For example, the fundamental error rate of memory devices based on some technologies may increase over time in response to degradation of an insulation layer. Accordingly, a level of redundancy that is appropriate for the fundamental error rate at the date of manufacture could be inadequate after a period of time. However, a level of redundancy that is appropriate at some date in the future might be excessive during the period of time the device was most likely to be used, immediately following manufacture (column 1, lines 45-55); Accordingly, it would be beneficial to develop a variable-length error correction code and method of use that dynamically alters the redundancy available to allow <u>substitution</u> of <u>a first ECC</u> with <u>a second ECC</u> <u>in response to changing error rates</u>, and which allows more efficient allocation of memory between payload and redundancy (column 2, lines 6-11); column 3, lines 28-36; see below for teaching by Yada et al.]; **and**

performing error correction code (ECC) calculations on the second segment according to a second ECC algorithm to encode the second segment [The fundamental error rate is particularly dependent upon factors that are a function of time. For example, the fundamental error rate of memory devices based on some technologies may increase over time in response to degradation of an insulation layer. Accordingly, a level of redundancy that is appropriate for the fundamental error rate at the date of manufacture could be inadequate after a period of time. However, a level of

redundancy that is appropriate at some date in the future might be excessive during the period of time the device was most likely to be used, immediately following manufacture (column 1, lines 45-55); Accordingly, it would be beneficial to develop a variable-length error correction code and method of use that dynamically alters the redundancy available to allow substitution of a first ECC with a second ECC in response to changing error rates, and which allows more efficient allocation of memory between payload and redundancy (column 2, lines 6-11); column 3, lines 28-36; see below for teaching by Yada et al.], **wherein the second segment is encoded substantially separately from the first segment** [figure 2, column 4, lines 16-31].

Regarding claim 1, Smith does not explicitly teach that **different ECC algorithms are used to encode different segments**.

However, Bassett et al. disclose in their invention "Error Correction Codes Applied Variably by Disk Zone, Track, Section, or Content" a method of applying different ECC algorithms to different sections of a memory storage device [For example, different error correcting codes of different strengths may be applied on a sector-by-sector basis, or on some other basis, depending upon the particular application, data types involved, and so forth (column 7, lines 29-33); the error correction selection criterion selects which of said first and second algorithms is to be applied in dependence upon the physical location of said data on said hard disk drive. In another embodiment, the error correction selection criterion selects which of said first and second algorithms is to be applied in dependence upon the type of said data to be written to the disk. The first and second error correction code algorithms

preferably produces a different number of error correction code bits for application to the data (column 2, lines 37-46); The method includes applying a first error correction code algorithm to a first set of data to be written to the hard disk drive. A second error correction code algorithm, different from the first, is applied to a second set of data to be written to the hard disk drive. The first and second error correction code algorithms may for example produce a different number of error correction code bits for application to said data. The selection between the first and second algorithms may be made, for instance, in dependence upon the physical location on the hard disk drive to which the data is to be written, or in dependence upon the type of said data to be written (column 2, lines 15-26); According to a preferred embodiment of the invention, the ECC encoder 40 can encode the data using more than one ECC. The ECC encoder 40 may, for example, provide two or more ECC coding strategies or algorithms by which the incoming data may be encoded. The selection of which particular strategy is used may depend upon a number of factors, below described in detail, depending, for example, on the radial location on the disk at which the data is to be written, the data type, and so on (column 3, lines 52-60); According to a preferred embodiment of the invention, it is observed that the need for error correction in many applications depends on the frequency and duration of soft errors, which, in turn, may depend upon the radial position of a given sector. Thus, two of the salient aspects of the invention are the need for an ECC for the duration and, frequency of soft errors and the need for an ECC for a given radial location (column 4, lines 37-45)].

Further Bassett et al. teach that the motivation of using different ECC algorithms to different blocks of memory instead of uniformly applying the same ECC algorithm to all blocks of memory is to save memory space [reducing the number of ECC bits that need be associated with at least some of the data to be written to the disk (12), the available space on the disk for user data can be increased (abstract)].

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize the benefits offered by applying different ECC algorithms to different sections of a memory device, as demonstrated by Bassett et al., and to incorporate it into the existing scheme disclosed by Smith, to further reduce the space required by ECC.

As to claim 2, Smith teaches that **the first segment includes the data area** [the payload portion (figure 2, 202)] **and the second segment includes the overhead area** [the redundancy portion (figure 2, 204)].

As to claim 3, Smith teaches that **the first segment includes a first section of the data area** [figure 2, 210] **and the second segment includes a second section of the data area** [figure 2, 208].

As to claim 6, Smith teaches that **dividing the at least part of the page into the at least two segments of the data includes:**

dividing the page into three segments, the three segments including the first segment, the second segment, and a third segment [a divider segregating the payload and redundancy portions may be dynamically relocated, thereby altering the size of the redundancy to allow for use of an error correcting code selected to provide

the data integrity required in response to changing conditions (abstract); figures 1 and 2 show the dividing of a memory page into a plurality of segments (206, 208, 210 and 212); column 4, lines 16-31].

As to claim 7, Smith teaches that **performing the ECC calculations on the third segment according to one of the first and second ECC algorithms to encode the third segment, wherein the third segment is encoded substantially separately from the first segment and the second segment** [The fundamental error rate is particularly dependent upon factors that are a function of time. For example, the fundamental error rate of memory devices based on some technologies may increase over time in response to degradation of an insulation layer. Accordingly, a level of redundancy that is appropriate for the fundamental error rate at the date of manufacture could be inadequate after a period of time. However, a level of redundancy that is appropriate at some date in the future might be excessive during the period of time the device was most likely to be used, immediately following manufacture (column 1, lines 45-55); Accordingly, it would be beneficial to develop a variable-length error correction code and method of use that dynamically alters the redundancy available to allow substitution of a first ECC with a second ECC in response to changing error rates, and which allows more efficient allocation of memory between payload and redundancy (column 2, lines 6-11); column 3, lines 28-36].

As to claim 8, Smith teaches that **the first segment includes a first section of the data area** [figure 2, 212]**, the third segment includes a second section of the**

data area [figure 2, 210], **and the second segment includes the overhead area** [figure 2, 214].

As to claim 9, Smith teaches that **the first segment includes a first section of the data area** [figure 2, 212], **the second segment includes a second section of the data area** [figure 2, 210], **and the third segment includes a third section of the data area** [figure 2, 208].

As to claim 11, refer to "As to claim 1."

As to claim 12, Smith teaches that **the memory system of claim 11 further including: a controller, the controller being arranged to process the code devices** [An application determination module 506 is adapted to determine the use to which the storage device 201 is to be put (column 6. lines 59-65); A code assignment module 508 is adapted to select an appropriate ECC from among those available in the ECC library 510, and also to select a level of redundancy required to accommodate information according to the code selected (column 7, lines 10-15); An error tracking, analysis and recording module 602 collects and records errors in the storage media (column 7, lines 45-47); A self-test module 604 provides a memory test that can thoroughly test the storage device 201 (column 7, lines 49-50); An age and use-tracking module 606 calculates the chronological age of the storage device 201 and the number of uses (column 7, lines 51-53); A storage application-tracking module 608 interfaces with the device or system within which the storage device 201 is installed, thereby allowing it to determine the use to which the storage device is being put (column 7, lines 57-59); the controller comprises all these modules].

As to claim 13, refer to "As to claim 2."

As to claim 14, refer to "As to claim 3."

As to claim 17, refer to "As to claim 6."

As to claim 18, refer to "As to claim 7."

As to claim 19, refer to "As to claim 8."

As to claim 20, refer to "As to claim 9."

As to claim 22, Smith teaches that **the code devices are one of software code devices and firmware code devices** [figure 7 shows the software procedure for calculating the ECC code for each page].

As to claim 23, refer to "As to claim 1."

As to claim 24, refer to "As to claim 2."

As to claim 25, refer to "As to claim 3."

As to claim 27, refer to "As to claim 6."

As to claim 28, refer to "As to claim 7."

As to claim 29, refer to "As to claim 8."

As to claim 30, refer to "As to claim 9."

8. Claims 4-5, 15-16, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith (US 6,961,890), in view of Bassett et al. (US 6,747,827), and further in view of Zhang et al. (US 6,662,333).

As to claim 4, neither Smith nor Bassett et al. explicitly mention that **the first ECC calculations are associated with an ECC algorithm is arranged to detect up**

to two incorrect bits and to correct up to one of the incorrect bits in each of the first segment and the second segment.

However, Smith does teach that the ECC library 510 typically contains a plurality of ECCs, including at least one weaker parity type code 512, at least one stronger BCH code 514, and at least one very strong Reed Solomon codes 516. To apply one of these ECCs to the redundancy 204 associated with the data structure 200, an appropriate divider similar to divider 206 may be selected to result in the required division between the payload and redundancy in the data structure 200 (column 7, lines 22-29).

Further, Applicants admit in the Background of the Invention Section of their disclosure that the above recited feature is well known in the art [some ECC algorithms that are used to encode and decode data for storage are known as 1-bit ECC algorithms and 2-bit ECC algorithms … (paragraph 0009)].

Moreover, Zhang et al. disclose in their invention “Shared Error Correction for Memory Design” an ECC scheme in which single bit errors are corrected and double bit errors are detected [column 1, lines 24-33].

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants’ invention to recognize that the particular limitation recited in this claim is well known in the art, as demonstrated by Applicants’ admission as well as Zhang et al., hence lacking patentable significance.

As to claim 5, Smith does not explicitly mention that **the ECC Algorithm is a Hamming Code ECC Algorithm**.

However, Smith does teach that the ECC library 510 typically contains a plurality of ECCs, including at least one weaker parity type code 512, at least one stronger BCH code 514, and at least one very strong Reed Solomon codes 516. To apply one of these ECCs to the redundancy 204 associated with the data structure 200, an appropriate divider similar to divider 206 may be selected to result in the required division between the payload and redundancy in the data structure 200 (column 7, lines 22-29).

Further, Zhang et al. teach in their invention "Shared Error Correction for Memory Design" that Hamming Code based ECC algorithms are well known in the art [a well known error correction code is the Hamming code (column 1, lines 55-67)].

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that the particular limitation recited in this claim is well known in the art, as demonstrated Zhang et al., hence lacking patentable significance.

As to claim 15, refer to "As to claim 4."

As to claim 16, refer to "As to claim 5."

As to claim 26, refer to "As to claims 4-5."

9. Claims 10, 21 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith (US 6,961,890), in view of Bassett et al. (US 6,747,827), and further in view of Kramer (US 6,182,239).

As to claims 10, 21 and 31, neither Smith nor Bassett et al. mention that **the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.**

However, the inventions of Smith are directly applicable to any type of flash memories, including NAND flash memory and MLC NAND flash memory.

Further, Kramer teaches in the invention "Fault-Tolerant Codes for Multi-Level Memories" a fault-tolerant code semiconductor flash memory storage devices including an array of individual multi-level cell (MLC) storage devices [abstract; column 2, lines 1-15] as well as NAND flash memory [column 2, lines 36-57].

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that the particular limitation recited in this claim is well known in the art, as demonstrated Kramer, hence lacking patentable significance.

10. ***Related Prior Art On Record***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Carnevale et al., (US 6,353,910), "Method and Apparatus for Implementing Error Correction Coding (ECC) in a Dynamic Random Access Memory Utilizing Vertical ECC Storage."
- Payne et al., (US 2003/0099140), "Data Handling System."
- Benton et al., (US 5,164,944), "Method and Apparatus for Effecting Multiple Error Correction in a Computer Memory."

- Sinclair et al., (US Patent Application Publication 2003/0156473), "Memory Controller."
- Moro et al., (US 6,769,087), "Data Storage Device and Method for Controlling the Device."
- Purdham, (US 5,666,371), "Method and Apparatus for detecting Errors in a System that Employs Multi-Bit Wide Memory Elements."
- Kellogg et al., (US 5,896,404), "Programmable Burst Length DRAM."

Conclusion

11. Claims 1-25 and 27-31 are rejected as explained above.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

October 12, 2006

PIERRE BATAILLE
PRIMARY EXAMINER
10/12/06